Q.P. Code: 16EC431 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Supplementary Examinations August-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Explain clearly about Moore's law.	**4M**
	b	Explain the different steps in n-well fabrication of CMOS transistor, with neat diagrams.	**8M**
		OR	
2		Analyze the different types of alternative pull-ups with neat sketches.	**12M**

UNIT-II

3	**a**	Explain 2µm based design rules with neat sketches.	**6M**
	b	Build a stick diagram and layout of NMOS inverter circuit. Both Input and Output points should be Polysilicon layer.	**6M**
		OR	
4	**a**	Develop the schematic and layout for 2-input NAND gate	**6M**
	b	Design the schematic and layout diagram of 2-input NOR gate using CMOS deign style.	**6M**

UNIT-III

5	**a**	What is pseudo NMOS logic?	**4M**
	b	Design the 2 input NAND gate by using pseudo NMOS logic.	**8M**
		OR	
6		Discuss the following below. Domino CMOS logic and NORA logic.	**12M**

UNIT-IV

7		Design a Arithmetic and Logic Unit circuit with four functions by using multiplexer logic.	**12M**
		OR	
8	**a**	Explain about different types of memory elements.	**6M**
	b	Construct the 4*4 array multiplier.	**6M**

UNIT-V

9	**a**	Discuss in details about CPLD structure and explain each block.	**6M**
	b	What is global routing? Discuss the advantages.	**6M**
		OR	
10	**a**	What is fault simulation?	**4M**
	b	Explain the stuck at 1 and stuck 0 faults with suitable diagrams.	**8M**

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